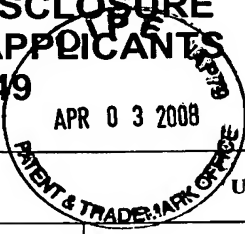


**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**



Attorney Docket No.  
2885/87

Serial No.  
10/501,903

Applicant(s)  
Vorbach

Filing Date  
March 1, 2005

Group Art Unit  
2193

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